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John Stattler	(Depositor's name)
<i>John Stattler</i>	(Signature)
2/11/2004	(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/854,146	05/11/2001	Jun Li	SPLX.P0050	6790

TITLE OF INVENTION: HIGH ACCURACY TIMING MODEL FOR INTEGRATED CIRCUIT VERIFICATION

APPLN. TYPE	SMALL ENTITY	ISSUE FEE	PUBLICATION FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	\$1330	\$300	\$1630	02/17/2004

EXAMINER	ART UNIT	CLASS-SUBCLASS
SIEK, VUTHE	2825	716-006000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

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1. Stattler
2. Johansen &
3. Adeli, LLP

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Cadence Design Systems, Inc. San Jose, CA

Please check the appropriate assignee category or categories (will not be printed on the patent); ☐ individual ☒ corporation or other private group entity ☐ government

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- ☒ Issue Fee
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